Nano-Semiconducting Devices Based Design of Voltage Controlled Oscillator

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF

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OF

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ELECTRICAL ENGINEERING

By

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NATIONAL INSTITUTE OF TECHNOLOGY

ROURKELA

CERTIFICATE

This is to certify that the thesis submitted by **Pankaj Prabhat** entitled, "**Nano-Semiconducting Devices Based Design of Voltage Controlled Oscillator**" in partial fulfillments for the requirements for the award of Bachelor of Technology Degree in Electrical Engineering at National Institute of Technology, Rourkela (Deemed University) is an authentic work carried out by him under my supervision and guidance.

To my knowledge, the matter embodied in the thesis has not been duplicated from any other University / Institute for the award of any Degree or Diploma.

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Department of Electrical Engineering
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The best aspect of presenting a thesis is the opportunity to show gratitude towards those who contributed to it. Unfortunately, no matter how extensive the list of people to be thanked is, it is always insufficient. Indeed this page of acknowledgment shall never be able to touch the horizon of generosity of those who tendered their help to me.

Last but not the least, our sincere thanks to all of our friends who have patiently extended all sorts of help in this project.

Pankaj Prabhat

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Abstract

Gordon Moore mentioned an exact objective fact in the 1960's that the quantity of gadgets on a chip duplicates like clockwork. The "Moore's Law" is a concise depiction of the persevering intermittent increment in the level of scaling down. Every time the base line width is lessened, we say that another innovation era or innovation hub is presented. Cases of innovation eras are 0.18µm, 0.13µm, 90nm, 65nm, 45nm… eras. The numbers allude to the base metal line width. Poly-Si door length may be littler. At each new hub, the different element sizes of circuit format, for example, the measure of contact openings, are 70% of the past hub. This routine of occasional size lessening is called scaling. Generally, another innovation hub is presented at regular intervals or somewhere in the vicinity

I have simulated various electronic circuits using CMOS in MATLAB, P-Spice, multi-sim (ICs used BS170, ZVP4424A) and Nano-CMOS using T-Spice where we can vary the physical dimensions of the MOSFET. The outputs were observed and the time delay was calculated. The above results showed that, as we go on reducing the size, the performance enhances

CHAPTER-2

INTRODUCTION

2.1 The MOSFET – Metal Oxide Field Effect Transistor

Although there is similarly assorted mixture of a JFET whose Gate terminal is electrically protected from the standard current conveying channel. This is known as an Insulated Gate Field Effect Transistor or IGFET. The to a great degree crucial kind of secured entryway FET which is in like manner secured which is utilized as a part of distinctive blends of electrical and electronic circuits. This is known as the (MOSFET) that is "Metal Oxide Semiconductor Field Effect Transistor". The IGFET or MOSFET varies from a JFET which is a voltage controlled field impact transistors it comprises of a "Metal Oxide" Gate cathode that is electrically isolated from the principle semiconductor N-channel or P-channel with a little and slight spread material which is by and large silicon dioxide, furthermore, that is fundamentally called as glass. This secured protection of the metal door terminal is gathered as a capacitor's plate. This partition of the entryway by which controlling happens makes the information limitation of the MOSFET more noteworthy in the Mega-ohms locale so it makes it practically unbounded. As we can see that the Gate end terminal is disconnected from the rule current containing port and like the JFET, the MOSFET furthermore carries on like a voltage resistor which can be controlled and that through the resistor current moving through the fundamental channel between the Drain and Source is generally related to the information terminal voltage. Also, similar to the JFET, the MOSFETs outstandingly more unmistakable delta limit resistance can basically aggregate more conspicuous measure of non-variable charge bringing on the MOSFET getting simply corrupted however if we handle it with thought it can be secured. Like the former JFET instructional activity, MOSFETs are basically devices with three terminal having a Gate, Drain and Source and we can see each of the P-channel (PMOS) and N-channel (NMOS) MOSFETs are moreover present there. The general difference this period is that MOSFETs are typically present in a few structures which are on a very basic level of two kinds:

1.1. Depletion Type – the transistor obliges the Gate-Source voltage, (VGS) to switch the gadget "OFF". The exhaustion mode MOSFET is identical to a "Regularly Closed" switch. MOSFETs image and its general setup are demonstrated as follows.

1.2. Enhancement Type – the transistor obliges a Gate-Source voltage, (VGS) to switch the gadget "ON". The improvement mode MOSFET is proportionate to a "Regularly Open" switch. The

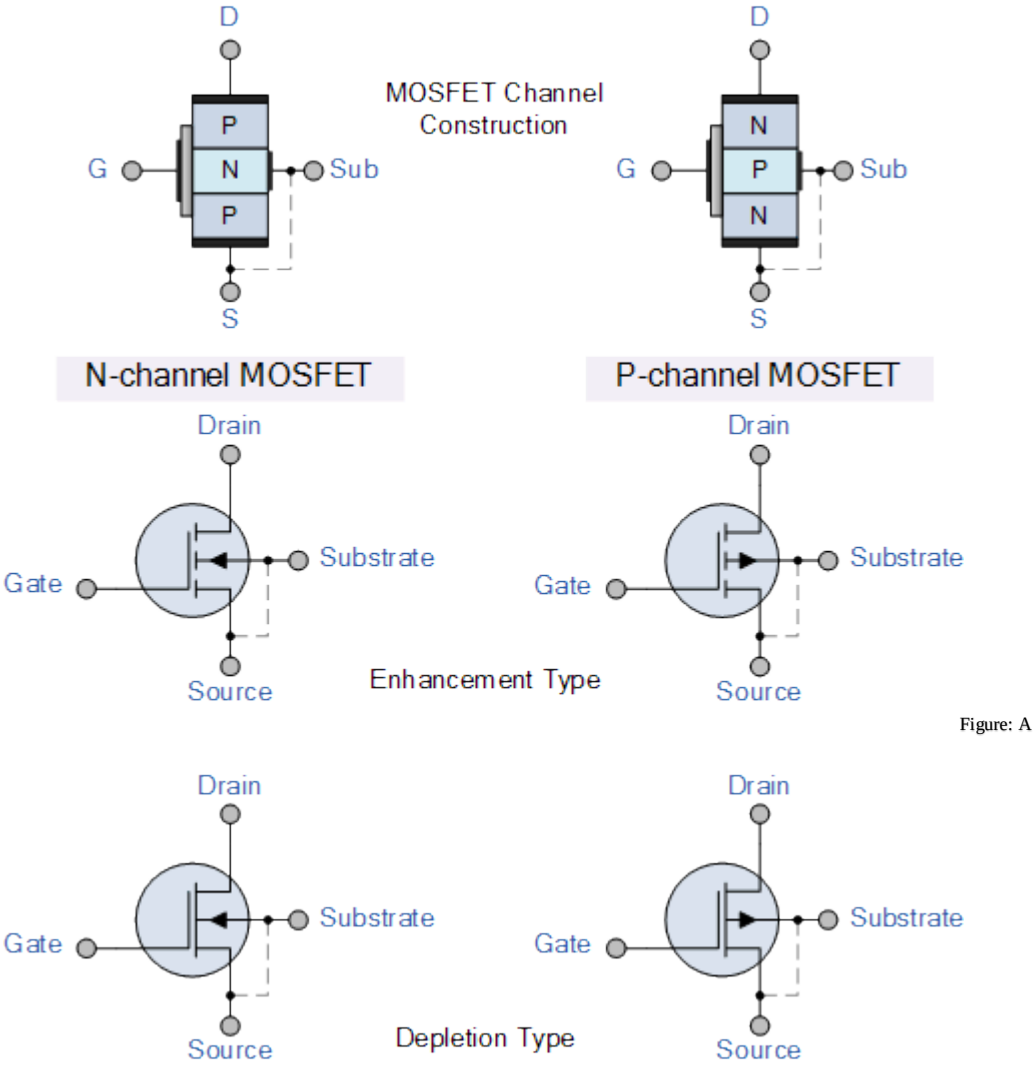

Figure: A

The MOSFET symbols which are indicated above tells us about an extra terminal called the Substrate and that is generally utilized neither an input nor an output circuit configuration but rather it is utilized for the substrate grounding. It makes connection to the main semi conductive port through a diode junction to its main body or the tab of the MOSFET made up of metal. Generally if we see certain discrete type of the MOSFET then we can see this substrate lead which id internally connected with the source port. If this would be the condition, as in enhancement categories which is usually eradicated for the symbol's clarity.

The semi conductive channel is represented by the line demarcating the drain and source interconnections. If we found a solid unbroken line then this shows us a "Depletion" (generally closed) categorized MOSFET and if we found the port line somewhat dotted or non-regular that is broken then that would be an "Enhancement" (generally open) categorized MOSFET. The way of the pointing of the cursor represents that that can be a P-channel or an N-channel device.

2.2 Basic MOSFET Structure and Symbol

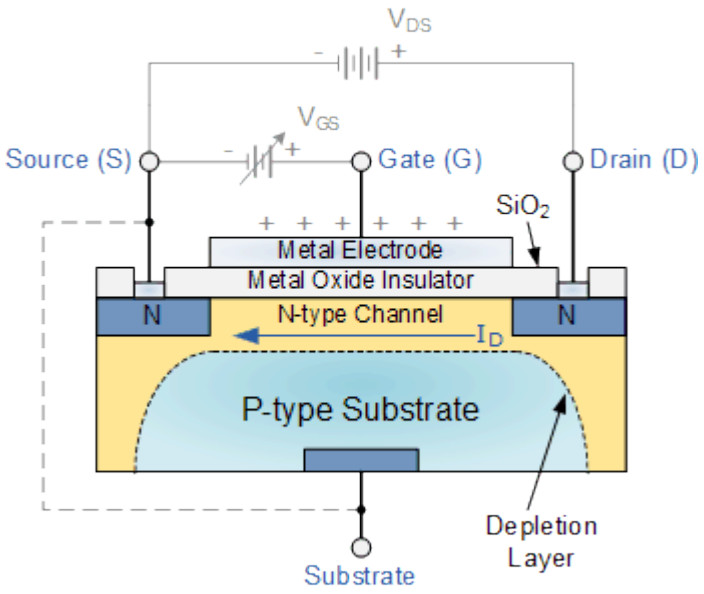

Figure: B

The model of the MOSFET is a bit dissimilar to that of the JFET. The electrodes of the gate that is positioned on upper layer of a very small and thin covering and we ca also get small N-type regions pair which is situated beneath the source and drain. The Enhancement and Depletion category of MOSFETs utilizes a filed generally electrical generated by a voltage of the gate to change the direction of charge carriers, N-channel electros or P-channel holes, with the semi conductive channel of drain-source.

. Due to the covered gate MOSFET equipment there is basically not any shortcomings which is applied which makes it totally practicable to bias the gate of a MOSFET in any polarity, either it is positive (+ve) or negative (-ve). We have seen in the foreseen example, that a junction field effect transistors gate, it must be somewhat not exact path to reverse-bias the PN-junction

So this is responsible for making this MOSFET device important like electrical or electronic devices such as switches or for making the logic gates because if we are taking the case of no bias the that are generally non conductible and this greater inlet restricting resistance which implies that a small amount or almost zero current is required as MOSFETs are devices that are voltage controlled. So the MOSFETs that are P-channel and the N-channel are present in basically two forms that are the Depletion type and Enhancement type.

Depletion-mode MOSFET

The Depletion-mode MOSFET, which is not so common than the enhancement categories which are generally on switched “ON” mode and this is also done by not affecting the usages of the voltage of a gate bias and putting it into a “normally-closed” mode device. Although, the voltage of a gate to source (V_{GS}) will put the equipment on “OFF” mode. Equivalent with the JFET categories. An N-channel MOSFET, a the channel got exuded by “positive” gate voltage ,which In turn maximizes the passing

of the drain current and thereby reduces or lessens the current of the drain current with respect to the voltage of the gate which comes down to negative and less.

If descried differently, then for an N-channel depletion mode MOSFET: $+V_{GS}$ will be having greater number of electrons and greater amount of current. But $-V_{GS}$ will be like reduced number of electrons and reduced amount of current. The reverse is also valid if we take the P-channel categories. Then a "normally-closed" switch will be equal to the depletion mode MOSFET.

2.3 Depletion-mode N-Channel MOSFET and circuit Symbols

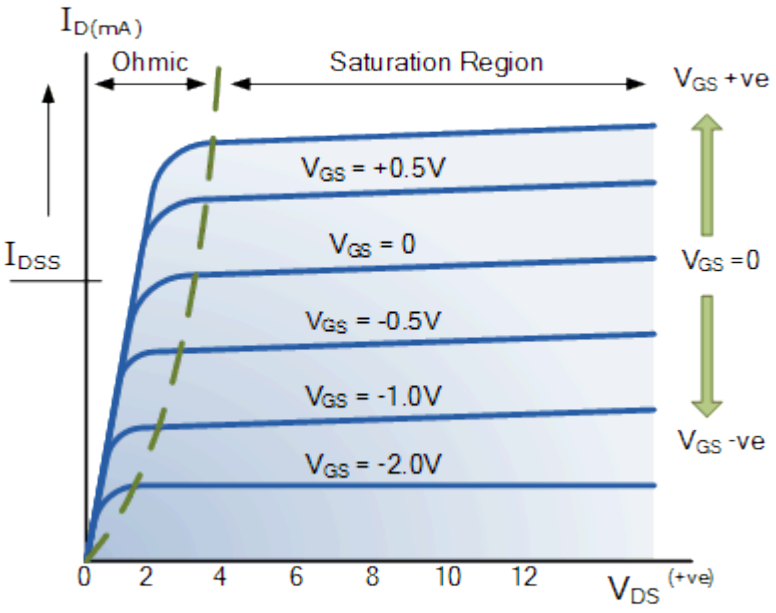

Figure: C

The depletion-mode MOSFET is made in an equivalent process to their JFET transistor's different parts were the drain-source port is previously conductive with the electrons and holes that are contained from the beginning within the channel having N-type or P-type. A conducting path having very little restriction is created by the intermixing of the channels between the Drain and Source with zero Gate bias.

2.4 Enhancement-mode MOSFET

The most basic Enhancement-mode MOSFET is actually the opposite to the depletion-mode category. The port which conducts is intermixed or it is sometimes not intermixed which will become Non-conductive. These all makes the equipment to go generally in "OFF" mode when the gate bias voltage is nearly equivalent or you ca say close to zero. A drain current can pass only if the voltage of a gate (VGS) is give in the terminal of the gate which should be at least more compared to the threshold voltage (VTH) level where this process takes place that is conductance happens which in turn makes it a device having the property of Trans conductance. The holes are pushed far due to this positive +ve gate voltage inside the port only which also attracts the electrons near the layer having oxides which maximizes the breadth of the port making the current to pass easily. This is the sole reason due to which this particular type of transistors are known as an enhancement categorized equipment and the channel is enhanced by this gate voltage. With the gradual increase in this voltage which is positive that will make the port restriction to get reduced more making the current of the drain gets increased ID through the channel. If we define it differently, then MESFET's N-channel: +VGS makes the transistor to go into the "ON" mode, but a zero or -VGS makes the transistor to go into "OFF" mode. So, the MESFET can be treated as a switch which is "normally-open

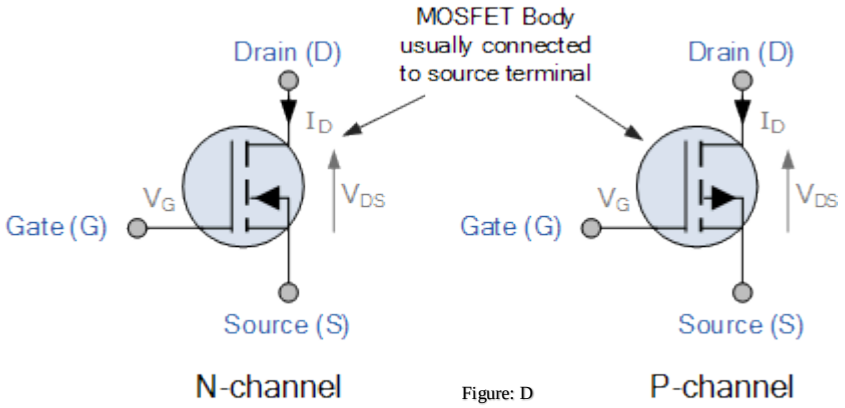

Figure: D

A fine electronic switch can be made by a MESFETs because of their less "ON" restriction and highly "OFF" restriction ad due to their extremely greater gate restriction that is it's resistance. MESFETs are generally utilized IC's for the production of CMOS categories *Logic Gates* and such circuits which utilizes power in the similar way as PMOS (P-channel) and NMOS (N-channel) gates. CMOS is basically abbreviated for *Complementary MOS* that means that the logic equipment's have PMOS and NMOS both their own design.

2.5 MOS-FET technology scaling

MOS ICs have satisfied the growing requirements of electronic devices for computing, entertainment, automation, communication with continued improvement in cost, operation speed, efficiency etc. It is now expected that this trend of rapid improvement will continue.

Technology Scaling

Since 1960's price of a bit of semi-conductor memory has dropped a 100 Million times and it continues. Similarly the prices of logic gates have shown a dramatic drop. This heavy drop in prices have encouraged new applications and semiconductor devices which has improved the ways people carry out almost all human activities. The primary engine that powered the development of electronics is the "miniaturization". By making the components and interconnects smaller more circuits can be fabricated on each silicon device and therefore each circuit becomes cheaper.

The fundamental accomplishment for presenting another innovation hub is the decrease of circuit size by 2. Since about twice the same number of circuits can be manufactured on every wafer with each new innovation hub, the expense per circuit is lessened fundamentally. That is the motor that drives down the expense of ICs.

Other than line width, some different parameters are likewise decreased with scaling, for example, the MOSFET gate oxide thickness and the power supply voltage. The diminishments are picked such that the transistor current density (Ion/W) increments with each new hub. Likewise, the littler transistors and shorter interconnects lead to littler capacitances. Together, these progressions cause the circuit deferrals to drop. Generally, coordinated circuit pace has expanded around 30% at each new innovation hub.

In summary, scaling improves cost, speed, and power per function with every new technology generation. All of these attributes have been improved by 10 to 100 million times in four decades --- an engineering achievement unmatched in human history! When it comes to ICs, small is beautiful.

Scaling Table

Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling	Constant Voltage Scaling with velocity saturation
Gate length	L	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate width	W	$1/\alpha$	$1/\alpha$	$1/\alpha$
Field	$\mathcal{E}$	1	α	α
Oxide thickness	t_{ox}	$1/\alpha$	$1/\alpha$	$1/\alpha$
Substrate doping	N_a	α^2	α^2	α^2
Gate capacitance	C_G	$1/\alpha$	$1/\alpha$	$1/\alpha$
Oxide capacitance	C_{ox}	α	α	α
Transit time	t_r	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha$
Transit frequency	f_T	α	α^2	α
Voltage	V	$1/\alpha$	1	1
Current	I	$1/\alpha$	α	1
Power	P	$1/\alpha^2$	α	1
Power-delay	$P \Delta t$	$1/\alpha^3$	$1/\alpha$	$1/\alpha$

TABLE: 1

CHAPTER-3

ANALYTICAL MODEL OF LOGIC GATES USING NANO-SCALE CMOS

Familiarization with basic circuits

Various logic gates viz. and or nor xor were simulated using matlab, p-spice and multisim

AND GATE:

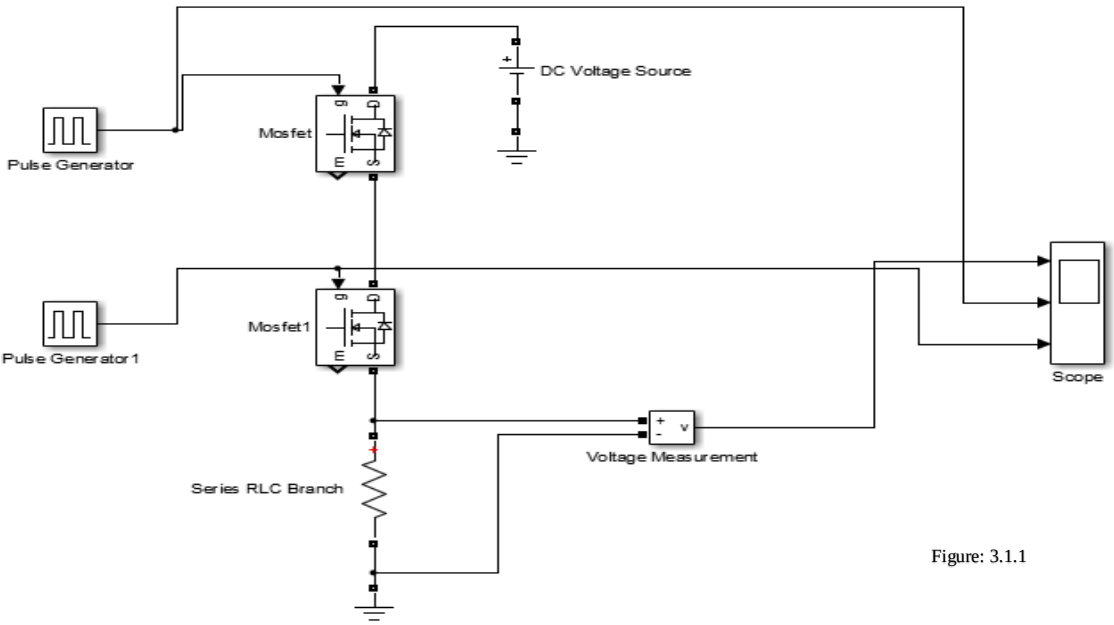

Figure: 3.1.1

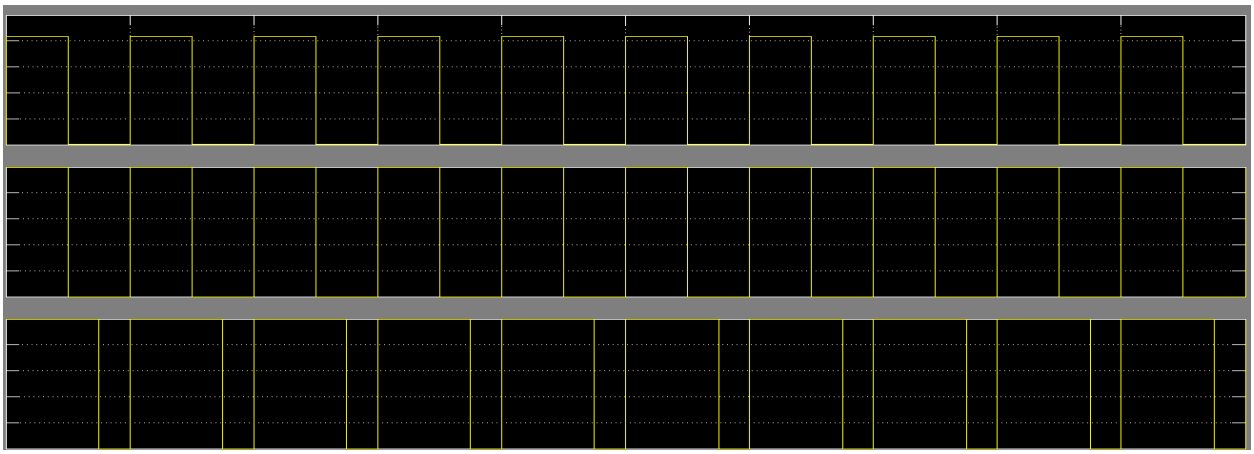

Figure: 3.1.2

OR GATE

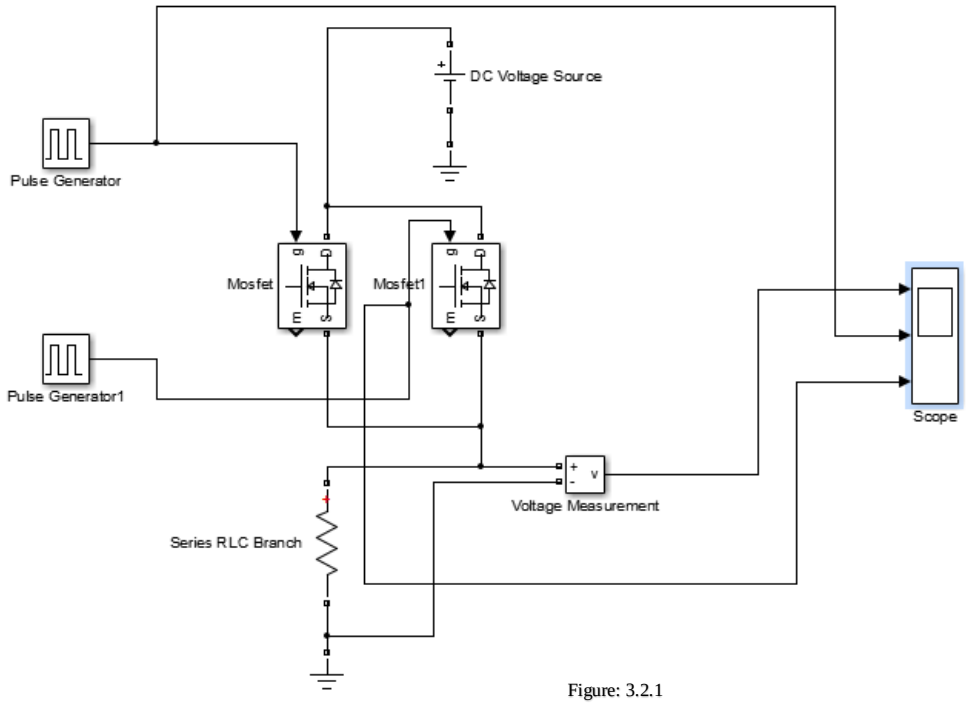

Figure: 3.2.1

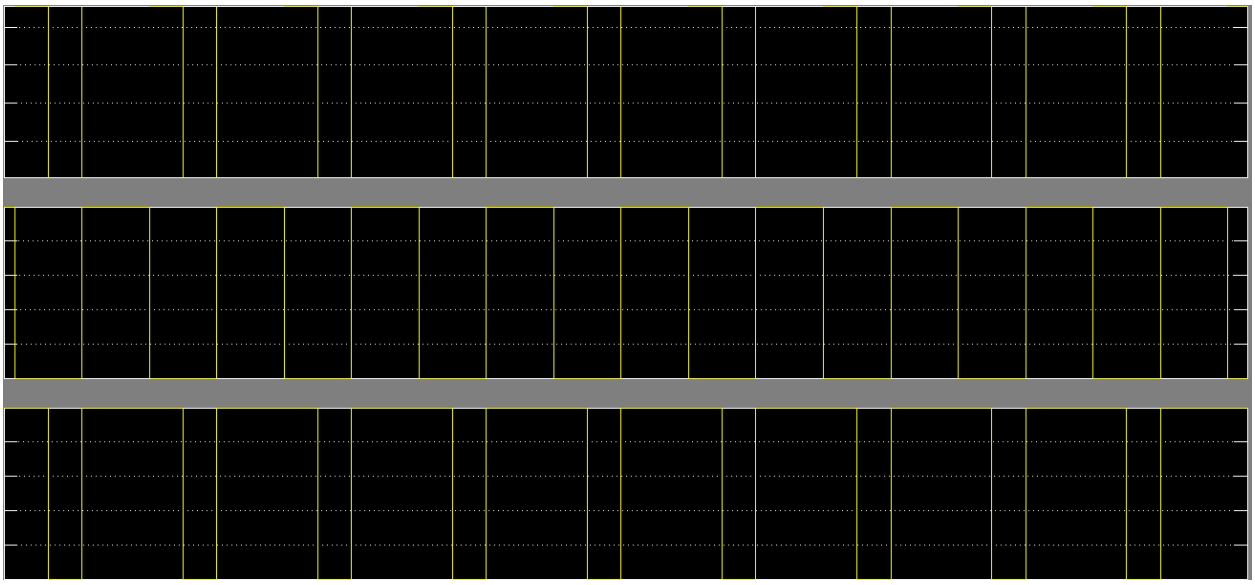

Figure: 3.2.2

Nor gate

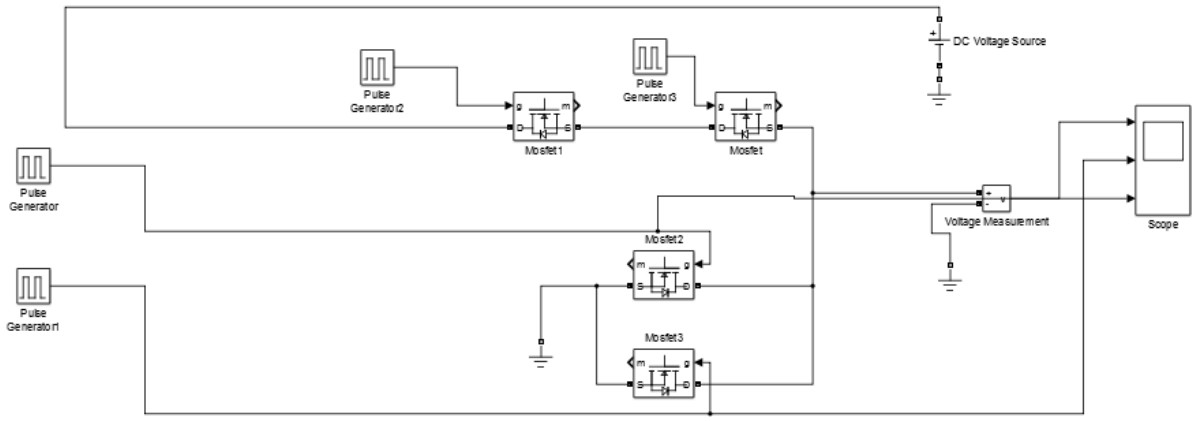

Figure: 3.3.1

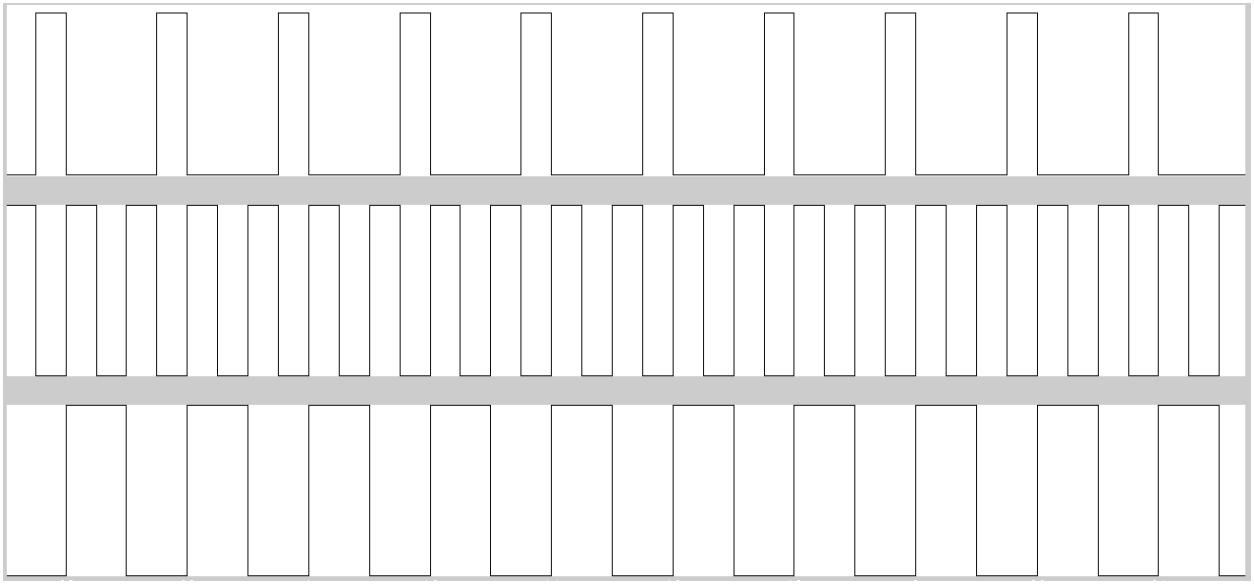

Figure: 3.3.2

XOR GATE

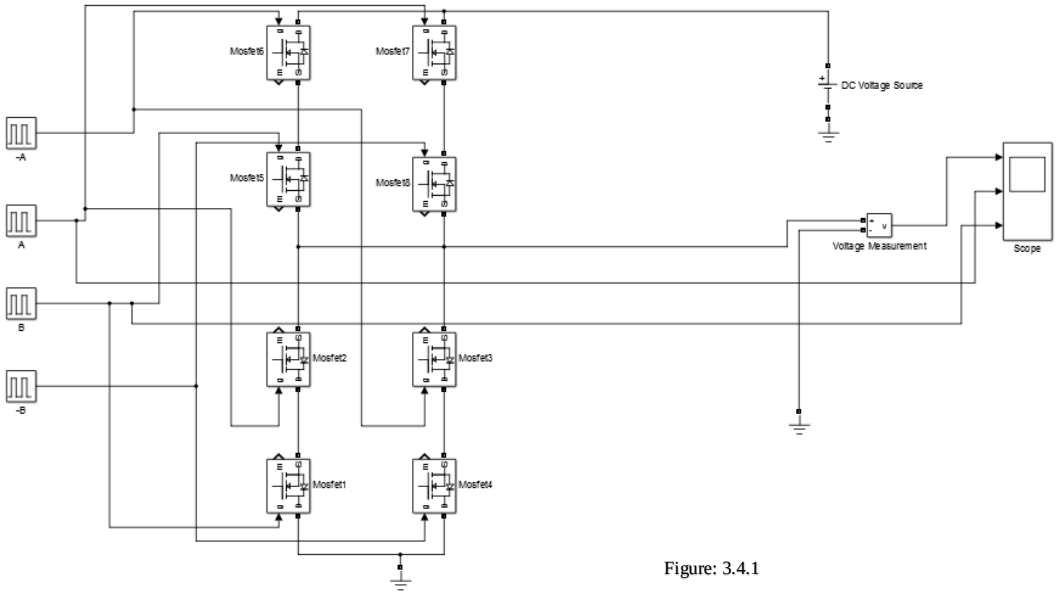

Figure: 3.4.1

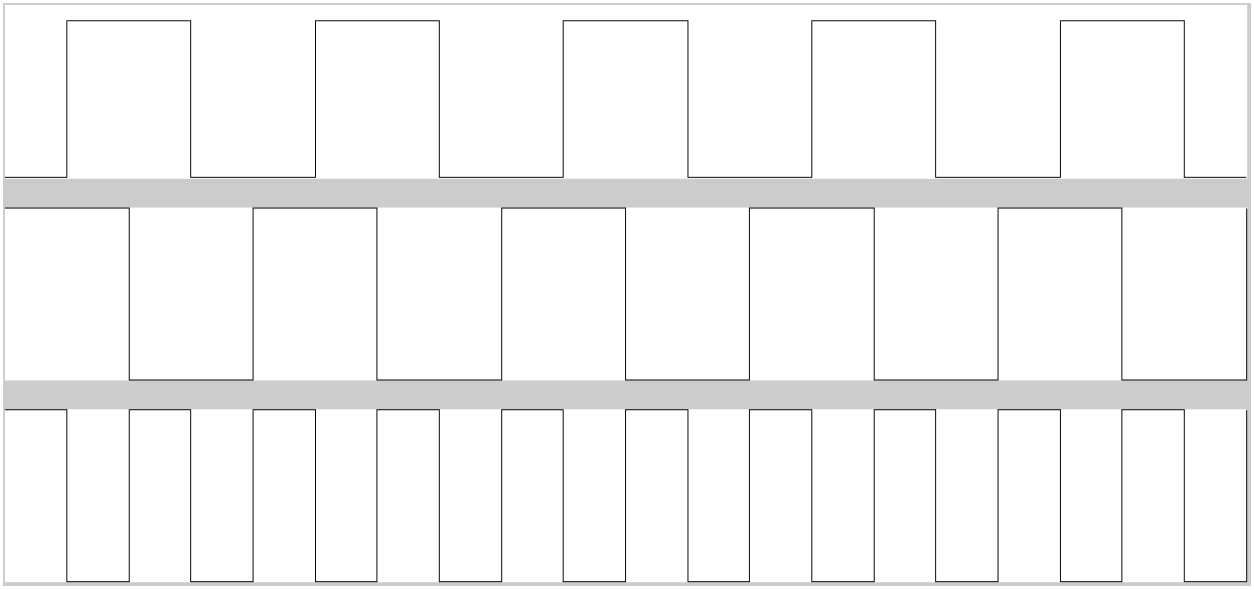

Figure: 3.4.2

Inverter

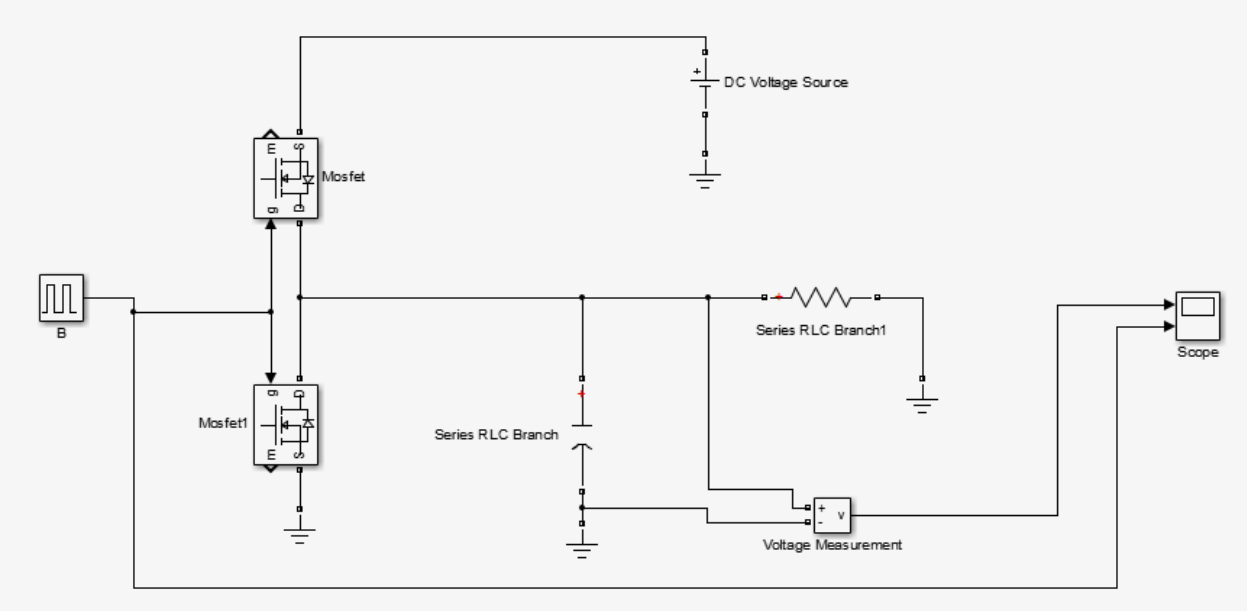

Figure: 35.1

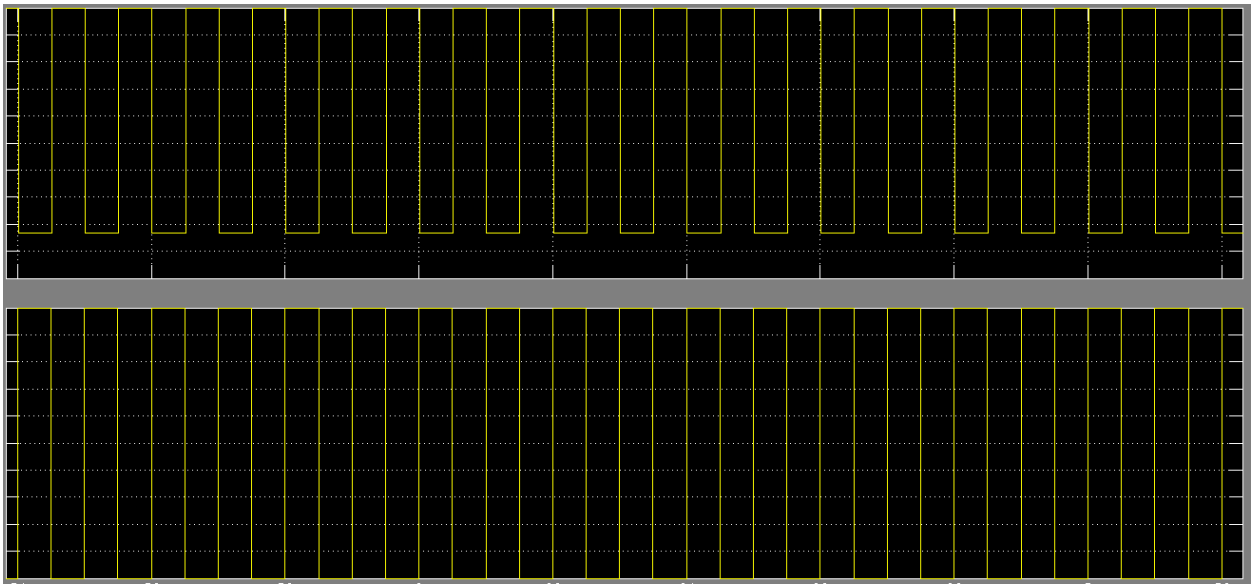

Figure: 3.5.2

CHAPTER-4

SIMULATION OF LGIC CIRCUITS (SEQUENTIAL AND COMBINATIONAL) USING NANO CMOS

Using the above above logic gates a few sequential and combinational circuits were designed at both conventional as well as nano scale

FULL ADDER CIRCUIT

A Full-Adder adds three one bit binary numbers (A B C) and gives output as two one bit binary numbers, a sum and a carry.

At conventional scale

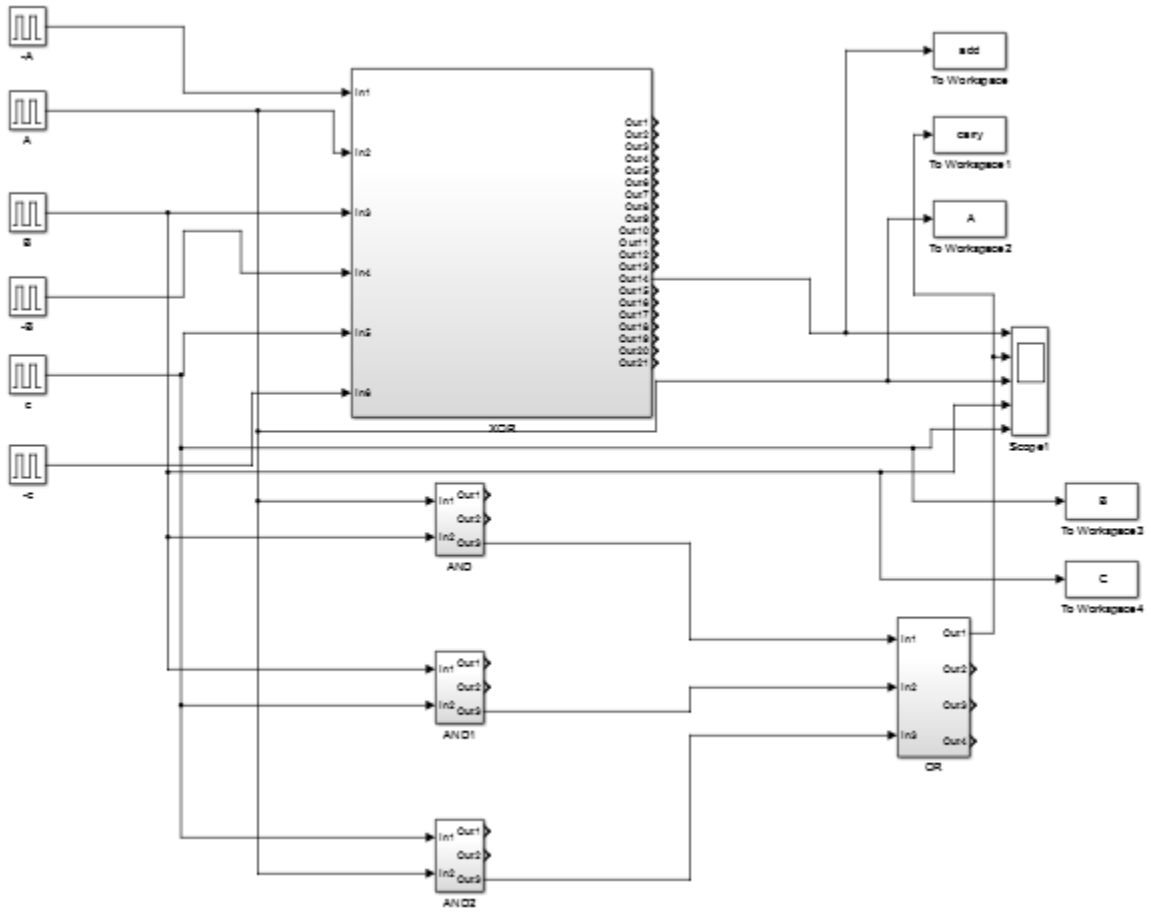

Figure: 4.1.1

Where the blocks represent various gates which are as follows:

XOR Gate:

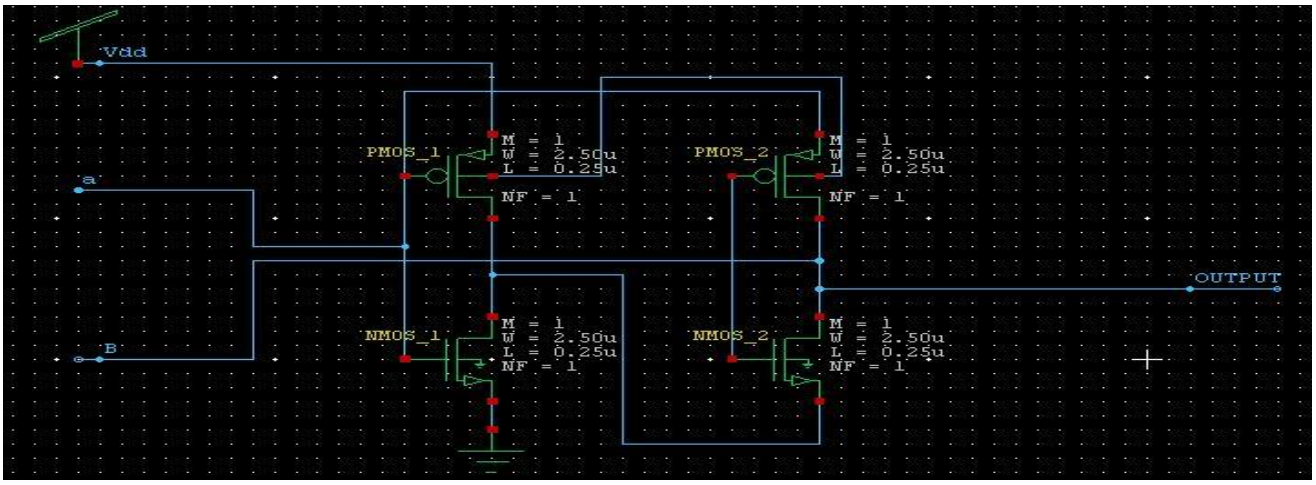

Figure: 4.1.2

AND Gate:

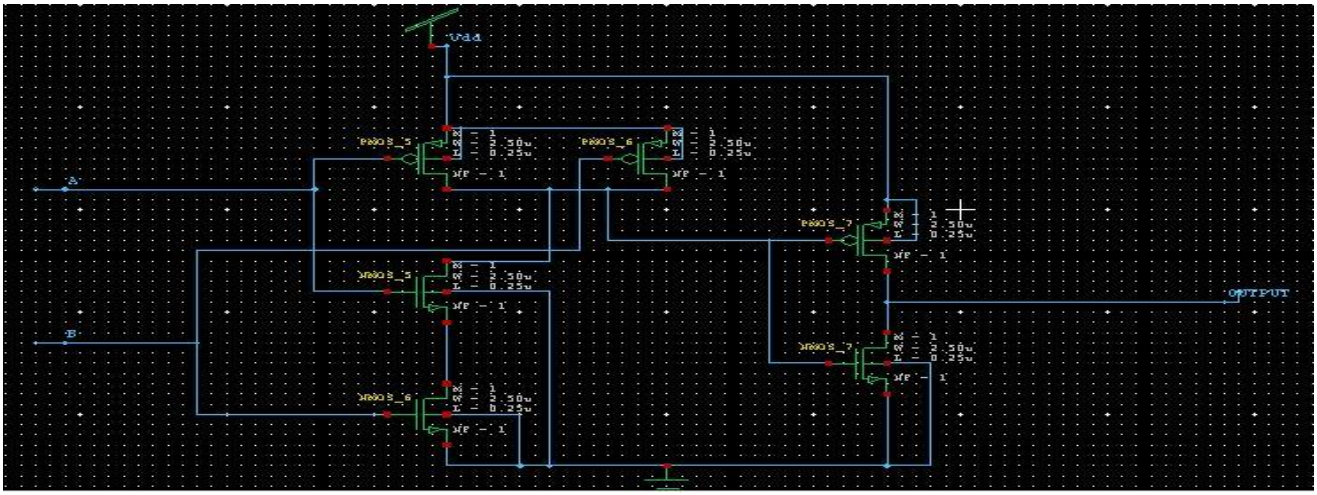

Figure: 4.1.3

OR Gate:

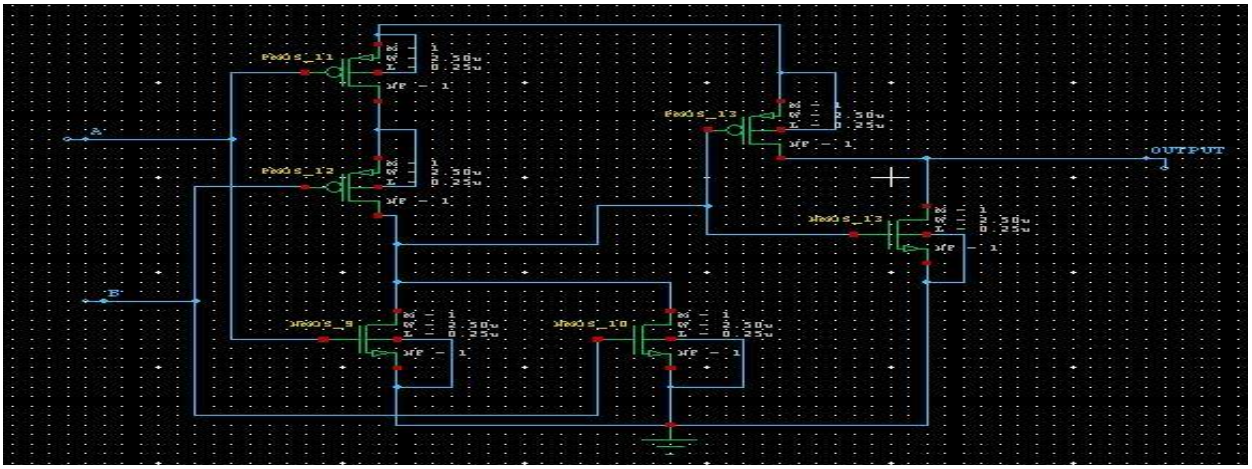

Figure: 4.1.4

Result:

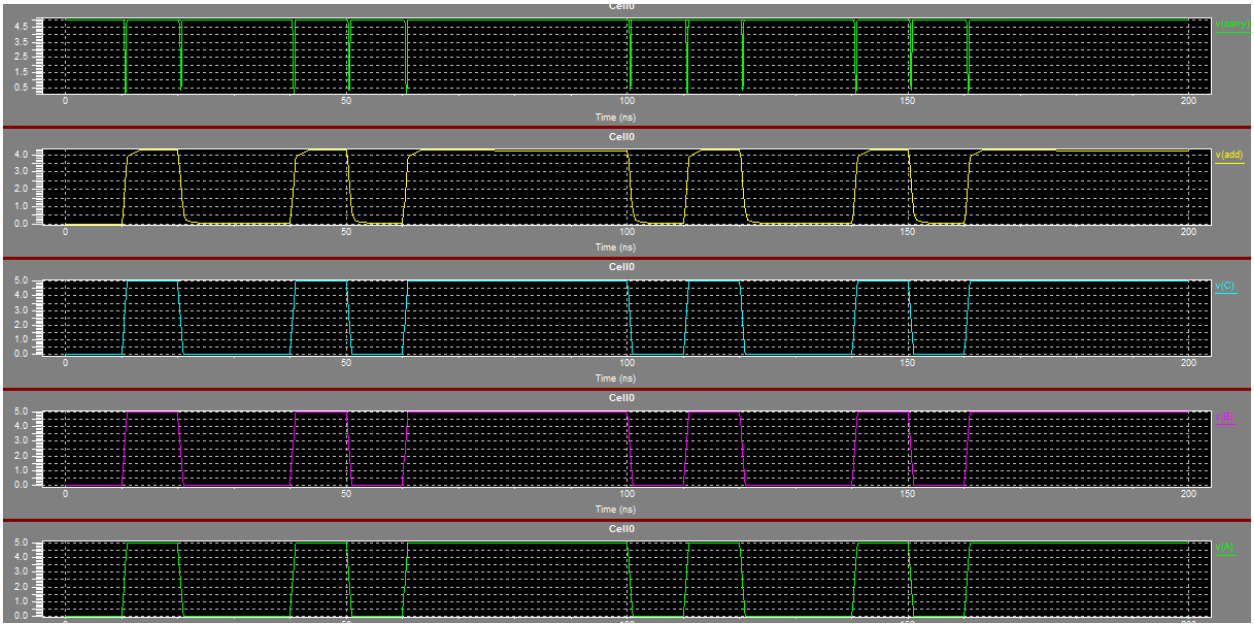

Figure: 4.1.5

Operating frequency: 100 MHz

Power consumption: 3.9uW

Propagation delay: 0.9nm

Multiplexer (4 to 1)

A Multiplexer is a device that chooses ones of many inputs by the help of select bit signals and forwards them into a single line.

At conventional scale :

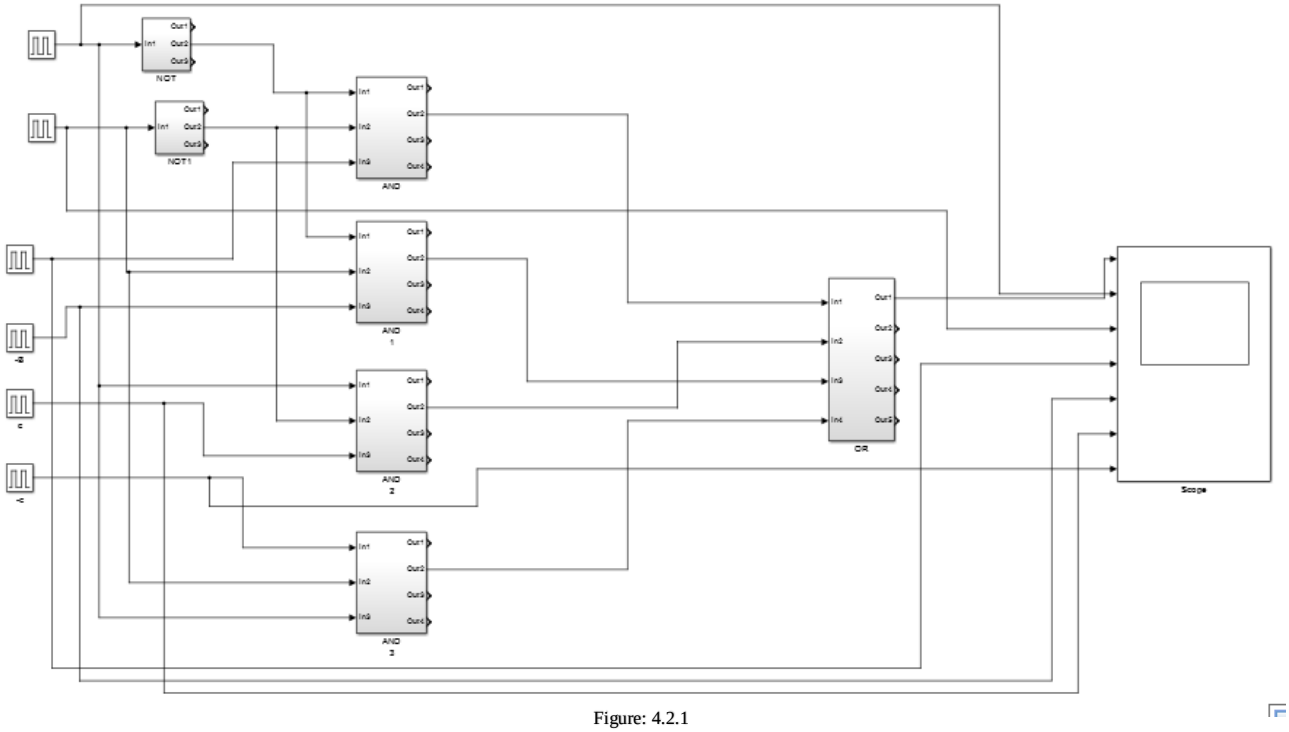

Figure: 4.2.1

Where the Blocks represent the Logic Gates as named which are shown below:

AND is constructed as shown below :

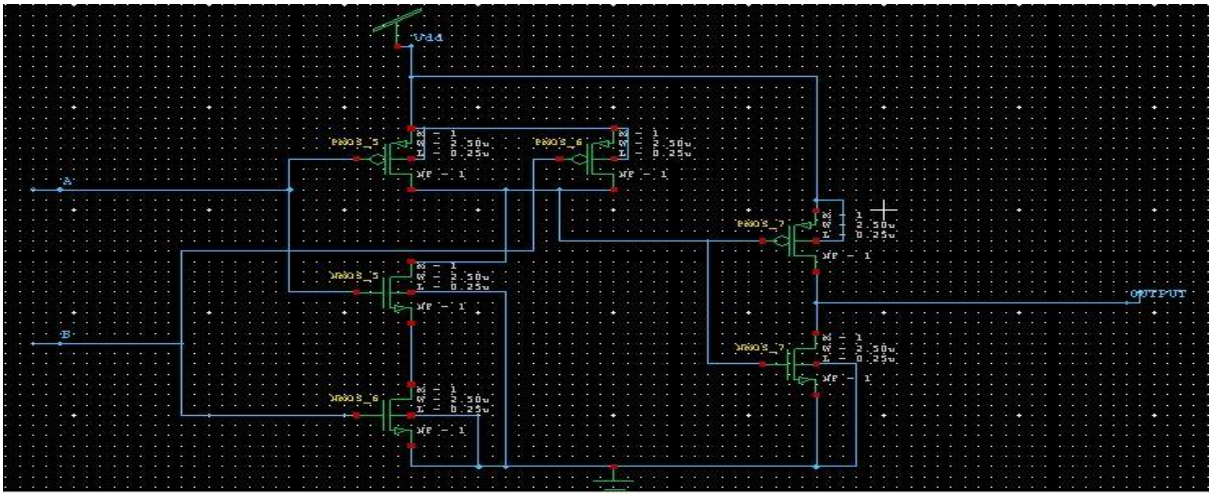

Figure: 4.2.2

OR Gate is constructed as shown below:

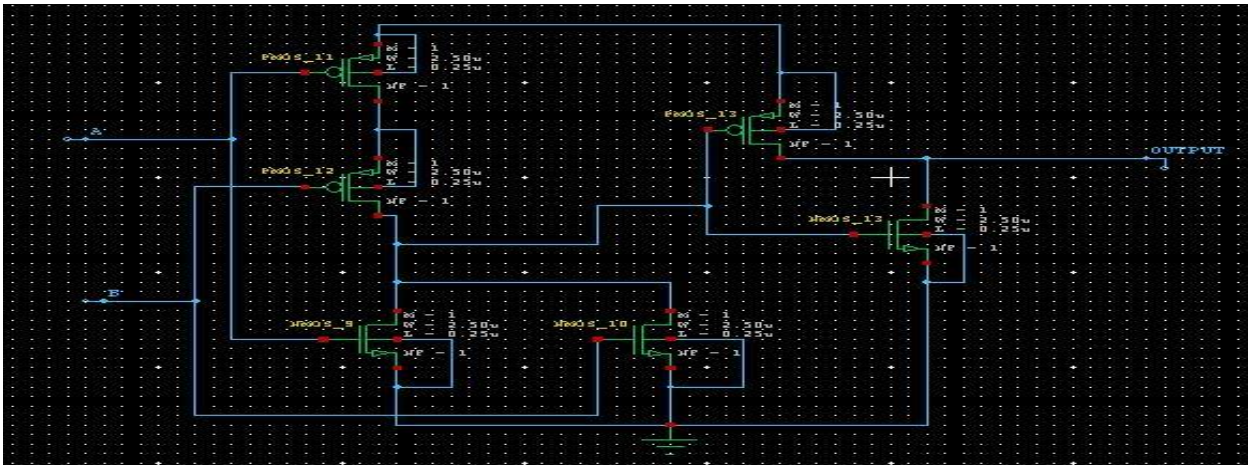

Figure: 4.2.3

Result:

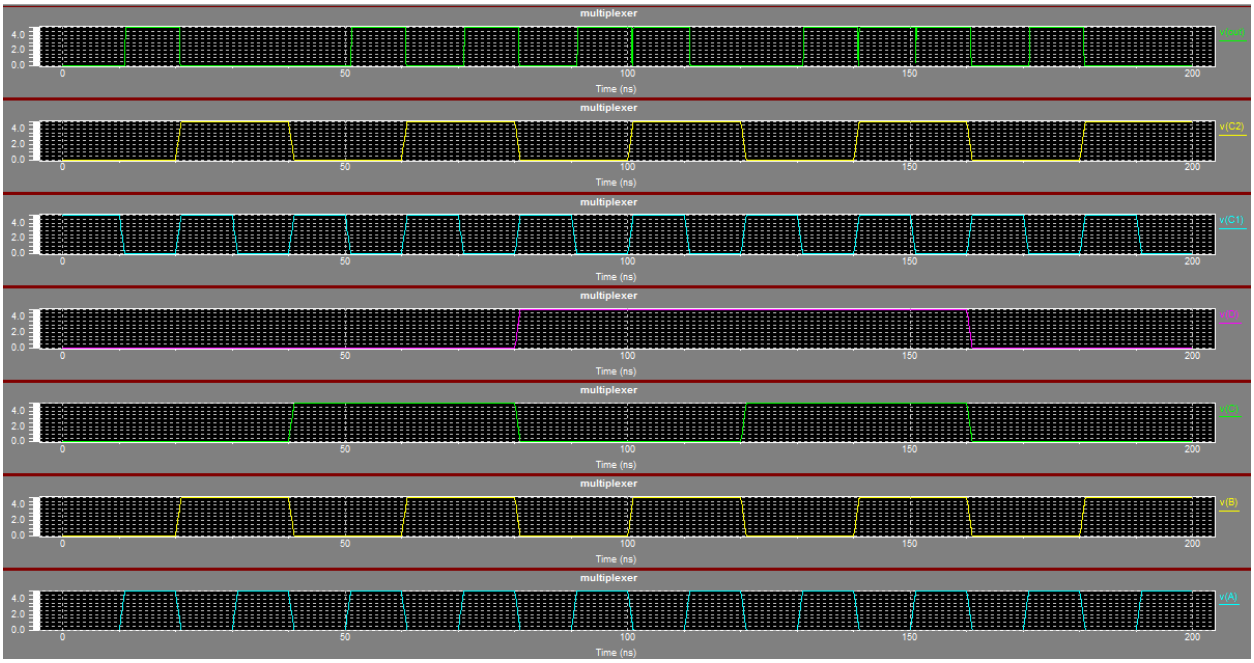

Figure: 4.2.4

Operating frequency: 100Mhz

Propagation delay: 1.9nm

Power consumption: 4.7uW 1.9nm

At reduced size :

Result:

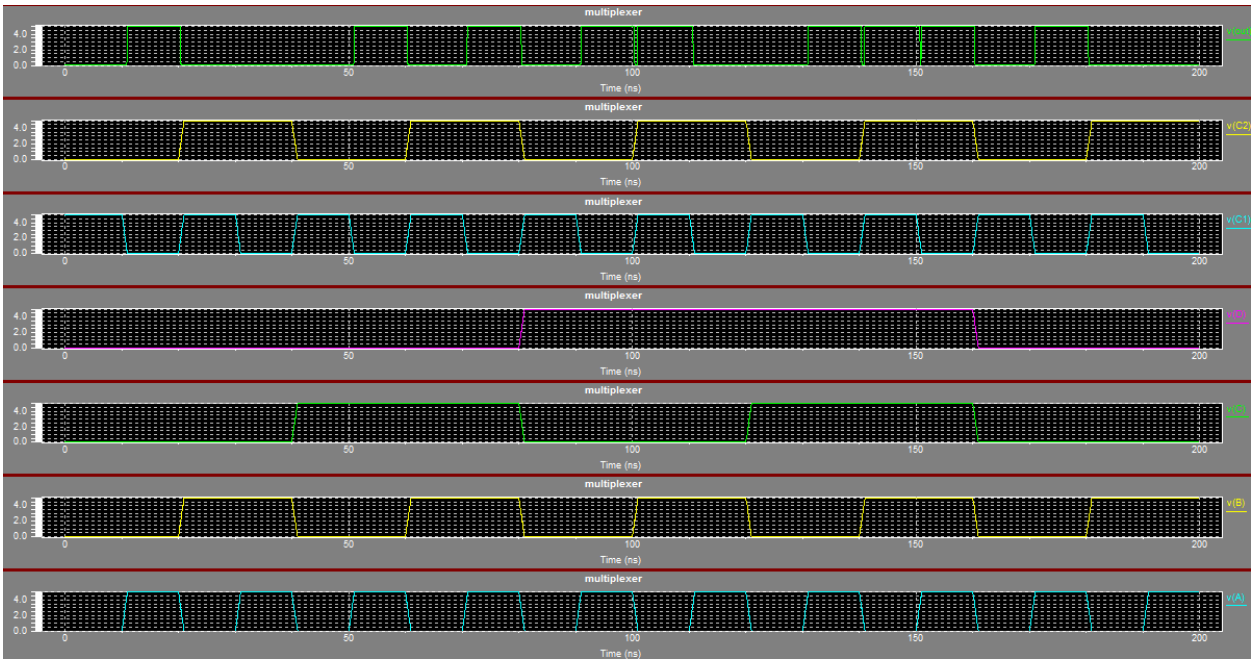

Figure: 4.2.5

Operating frequency: 100Mhz

Propagation Delay: 1.6nm

Power consumption: 4.1uW

SR Flip Flop:

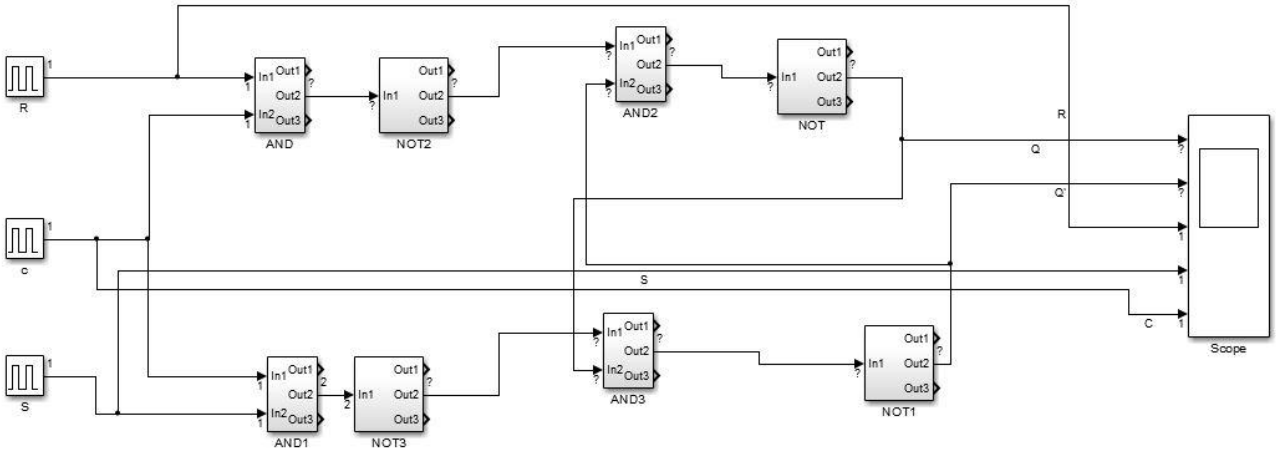

Figure: 4.3.1

Where the blocks represent the logic gates as named:

AND Gate:

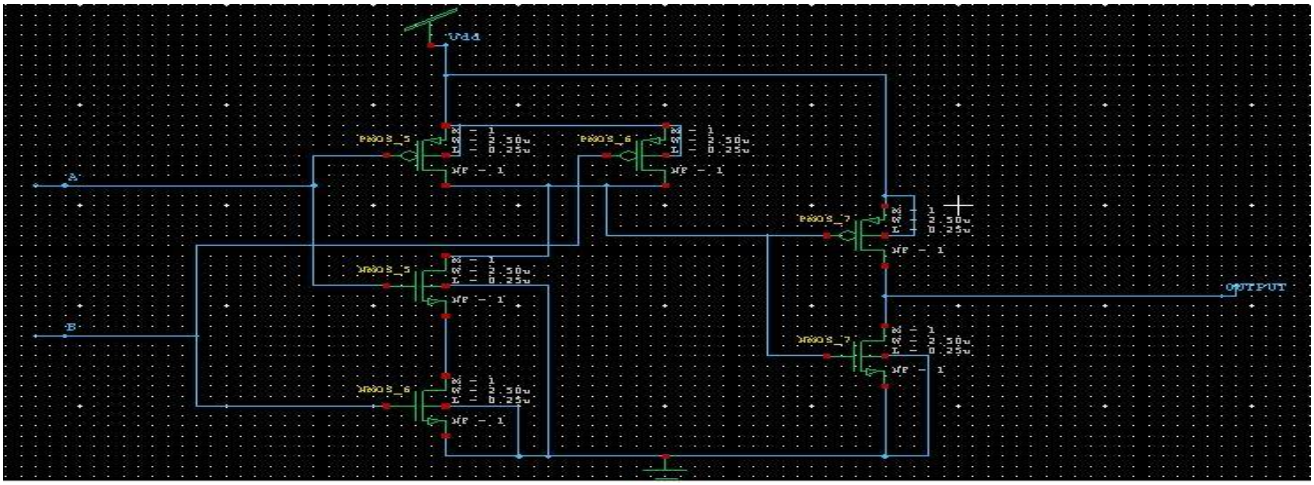

Figure: 4.3.2

NOT Gate:

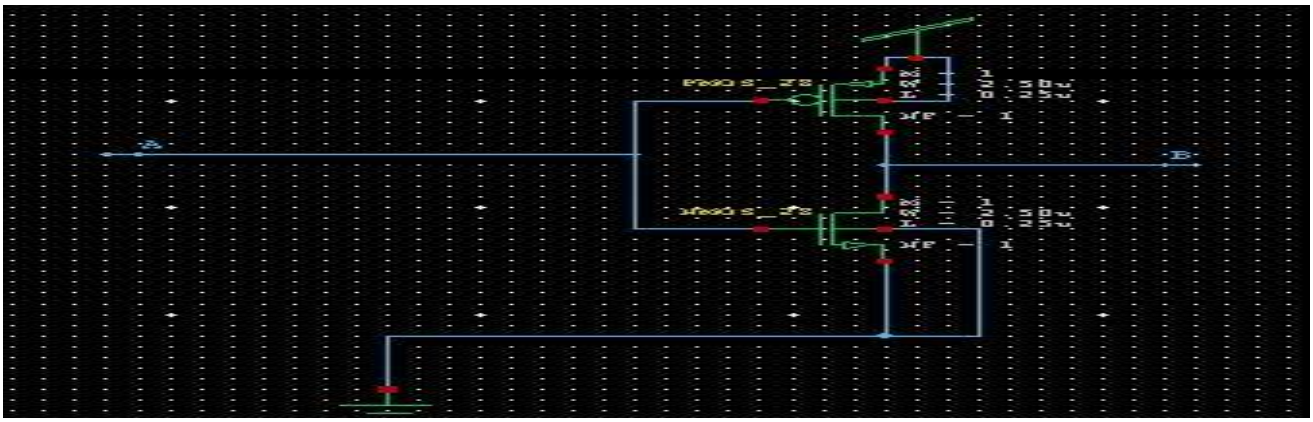

Figure: 4.3.3

Result:

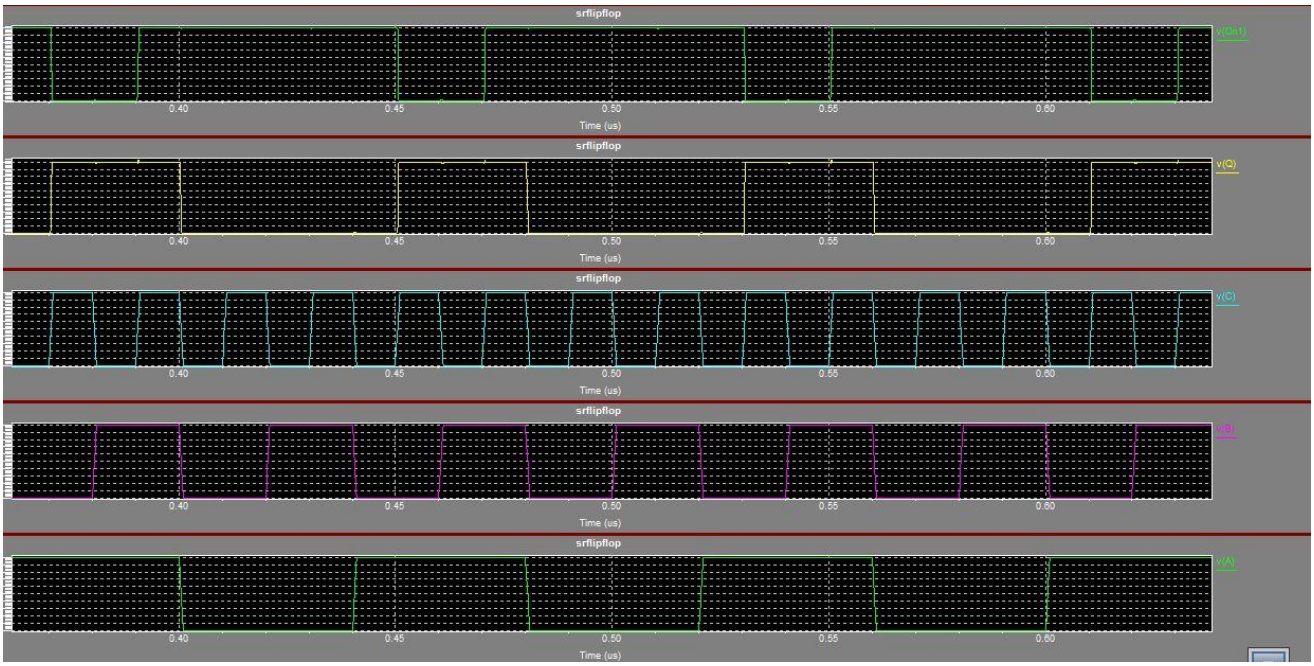

Figure: 4.3.4

Operating frequency: 100Mhz

Power consumption: 4.7uW

Propagation delay: 3.6nm

CHAPTER-5

PERFORMANCE ANALYSIS AND COMPARISION

Comparisions:

TABLE: 2

	Conventional size			Nano scale (2.5u x 250n)			Nano scale (1.25u x 125n)		
	Operating Frequency	Propagation Delay	Power Consumption	Operating Frequency	Propagation Delay	Power Consumption	Operating Frequency	Propagation Delay	Power Consumption
Multiplexer	5 Mhz	0.08um	0.21 mW	100Mhz	1.9nm	4.7uW	100Mhz	1.6nm	4.1uW
Full adder	5 Mhz	0.05um	0.18 mw	100Mhz	0.9nm	3.9uW	100Mhz	0.6nm	2.8uW
SR Flip Flop	5 Mhz	0.04um	0.36 mw	100Mhz	5.6nm	4.4uW	100Mhz	4.3nm	3.6uW

CONCLUSION:

Each nano-scale transistor was observed to be consuming lesser power with respect to conventional counterparts thus higher efficiency. Reduction in propagation delay was also noticed. So, it could be concluded that downsizing of MOSFET results in:

1) Reduced capacitance.

2) Reduced switching time of MOSFET.

3) Reduced power consumption.

4) Increase in number of transistors.

5) Increased functionality.

6) Increase Circuit Operation Speed.

Thus downscaling of Si devices is very essential and it very much enhances the performance of the device in terms of power consumption, speed, etc.

CHAPTER- 6

FUTURE WORK

Applications

Some of the Nano-CMOS are DG-MOSFET, FinFET, DG-FinFET, ultra-small MOSFETs, SiGe HBTs. These can be used for different applications in the world of electronics, such as SD-RAM and Processors, etc. and also in mobile technology.

It is also used in Low Power Applications of CMOS circuits.

It is additionally utilized as a part of Low Power Applications of CMOS circuits. Thus, the Nano-Technology based MOSFET supplant the mass CMOS and will make the PC time quicker and more dependable. It will acquire insurgency the universe of correspondence and gadgets, as everything is digitalized and relies on upon transistors. Indeed, even a little advanced clock needs clock circuits for its operation furthermore a PC processor, RAM etc. they excessively require transistor for operation.

Nano-Scale Mos's preferences over mass MOS are, it is little in size, low power consuming, quick working, and it additionally has same manufacture transform as a MOSFET. FinFET being little in size, all the more no can be created in a solitary IC chip. Furthermore, works are going ahead to make the transistor in Nano run to check a portion of the issues created by little scaling, for example, Power Density, temperature and so on.

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